

## NOVEL SYNTHESIS METHODOLOGY FOR CONTROLLING ZERO-CURRENT ZERO-VOLTAGE TRANSITION DC/DC BOOST CONVERTER.

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### Abstract

Among the soft-switching techniques, the Zero-Current Zero-Voltage Transition (ZCZVT) technique is used in this paper. It is based on the Resonant Transition Mechanism requirements, which permit newcomers to perceive the Resonant Transition techniques as a whole instead of dissimilar soft-switching techniques. The open loop operation of the power circuit (DC/DC Boost Converter) and control circuit have been implemented and tested with MatLab software. The simulation test facility and the analytical development tools being used are described. The derivation of closed loop control strategy based on fuzzy logic control with nonlinear fuzzy sets for input and output variables is described in detail. The closed loop simulation results that describe the performance of the proposed converter with this control strategy due to different effects are also included.

طريقة جديدة للسيطرة على مغير تيار مستمر إلى مستمر نوع (ZCZVT) رافع للفولتية ذو تقنية الانتقال الرنيني

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### الخلاصة

من بين تقنيات القدح الناعم اعتمد هذا البحث تقنية الانتقال عند التيار الصفري والفولتية الصفرية (ZCZVT) والتي تعتمد بدورها ميكانيكية الانتقال الرنيني والتي تسمح باستخدام نوع من القدح الناعم يعتمد الانتقال الرنيني كبديل متكامل عن ما هو معروف من تقنيات القدح الناعم الأخرى. استعملت برامجيات MATLAB لغرض تمثيل وفحص اداء المغير المقترح تحت تأثير نوعين من دوائر السيطرة (المفتوحة والمغلقة). تم تصميم دائرة سيطرة مغلقة اعتمدت تقنية السيطرة المضبية ذات الاجاميع الغير خطية لوصف متغيرات الادخال والايخراج لغرض فحص اداء المتغير لانواع مختلفة من التاثيرات، وقد اظهرت النتائج التي تم الحصول عليها نجاح دوائر السيطرة في استيفاء شروط العمل المطلوبة للمغير المستخدم.

overlapping of voltage and current result in high switching losses (see Fig.2-a).

The soft switching techniques aim to reduce the mentioned overlap between voltage and current during the commutation (see Fig.2-b). Thus it is possible to reduce switching losses, enabling high power density, with reduced audible noise, volume and weight of filters, as well as high output voltage quality [7].

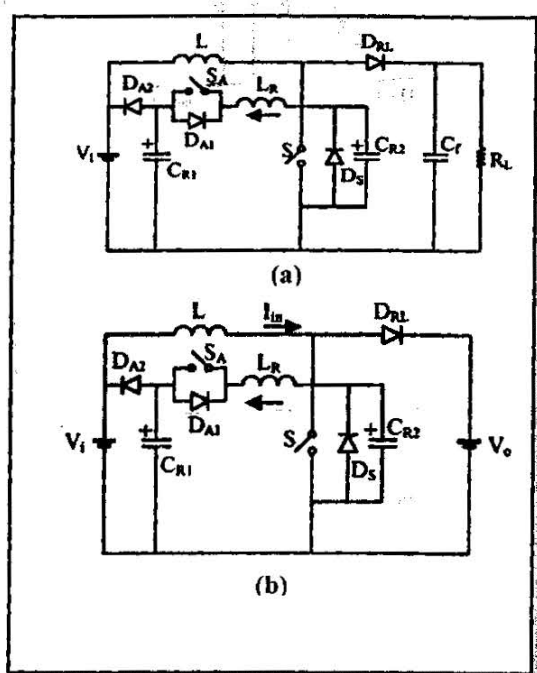


Fig.1 ZCZVT PWM Boost Converter.

- (a) Circuit diagram, and  
(b) Simplified diagram.

## 2.1 Operation Principles

To simplify the analysis, the input current and voltage are considered constant during one switching cycle (see Fig.1-b). There are fourteen operating stages during

one switching cycle as can be seen in Fig.3 [8], insuring the achievement of the following main features of the used topology as:

- ❖ There are no additional voltage stresses on power semiconductor devices.
- ❖ Commutation under ZCS and ZVS at both turn on and turn off for main switch.
- ❖ Commutation under ZCS at turn on and under ZCS and ZVS at turn off for the auxiliary switch.
- ❖ The output rectifier  $D_{RL}$  is commutated under ZVS and its reverse recovery is minimized.
- ❖ The commutation cell is placed out of the main path, and it is activated during the switching transition only.

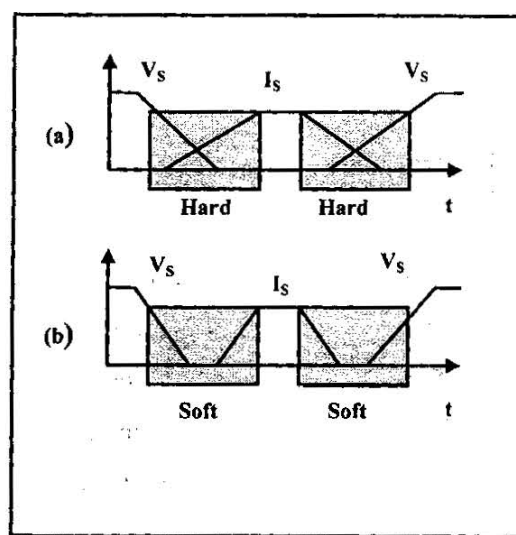


Fig.2 The switching process  
(a) Hard, and (b) Soft

## 1. Introduction

In recent years there has been a growing interest by the industry in high frequency and small size switched power converters. For this reason, an ever growing number of new topologies have been proposed in the literature. Most of them promise higher performance, efficiency and power density.

One efficacious way to obtain high efficiency converters is to employ some soft-switching technique to the power converter stage, which makes use of auxiliary components (passive and active) to limit the  $di/dt$  and/or  $dv/dt$  during the commutation process and minimize the overlap between voltage and current waveforms through the switching device, thus reducing its switching losses. In some cases, the auxiliary devices shape the voltage and/or current waveforms in such way, that the current and voltage overlapping through the device is quite reduced [1-4]. Although many soft-switching techniques can really improve the converter performance, the **Soft-Transition Technique** is one of the most well succeeded and consolidated technique in the state-of-the-art of soft-switching [5,6]. It is capable to provide a wide load range under soft-switching conditions with low, or even no, additional stresses on main semiconductor devices and very low stresses on auxiliary devices. These

characteristics are obtained due to the unique location of the auxiliary circuit that is indeed in parallel with the main power path. Additionally to the location, the auxiliary circuit is activated only during a small interval surrounding the main switch(es) commutations.

In order to contribute in the development of the Resonant Transition converters, mainly for the Zero-Current Zero-Voltage Transition techniques (**ZCZVT**), this paper presents a new methodology to control the Resonant Transition mechanism for one class of DC-DC converters (**boost converter**). The present result show that the open and closed loop control circuits can achieve the soft-switching of the used main and auxiliary switches and in the same time improving the output voltage quality.

## 2. The ZCZVT PWM Boost Converter

Fig.1-a shows the ZCZVT commutation cell applied to a PWM boost converter [8]. It is a shunt resonant network activated during the switching transitions only. The main goal of the commutation cell is to convert the commutation of converter semiconductor devices from the **hard** switching to the truly **soft** switching. With **hard** switching the devices change their states while they are subjected at bout finite current and voltage values so that, high switching stresses produced by the

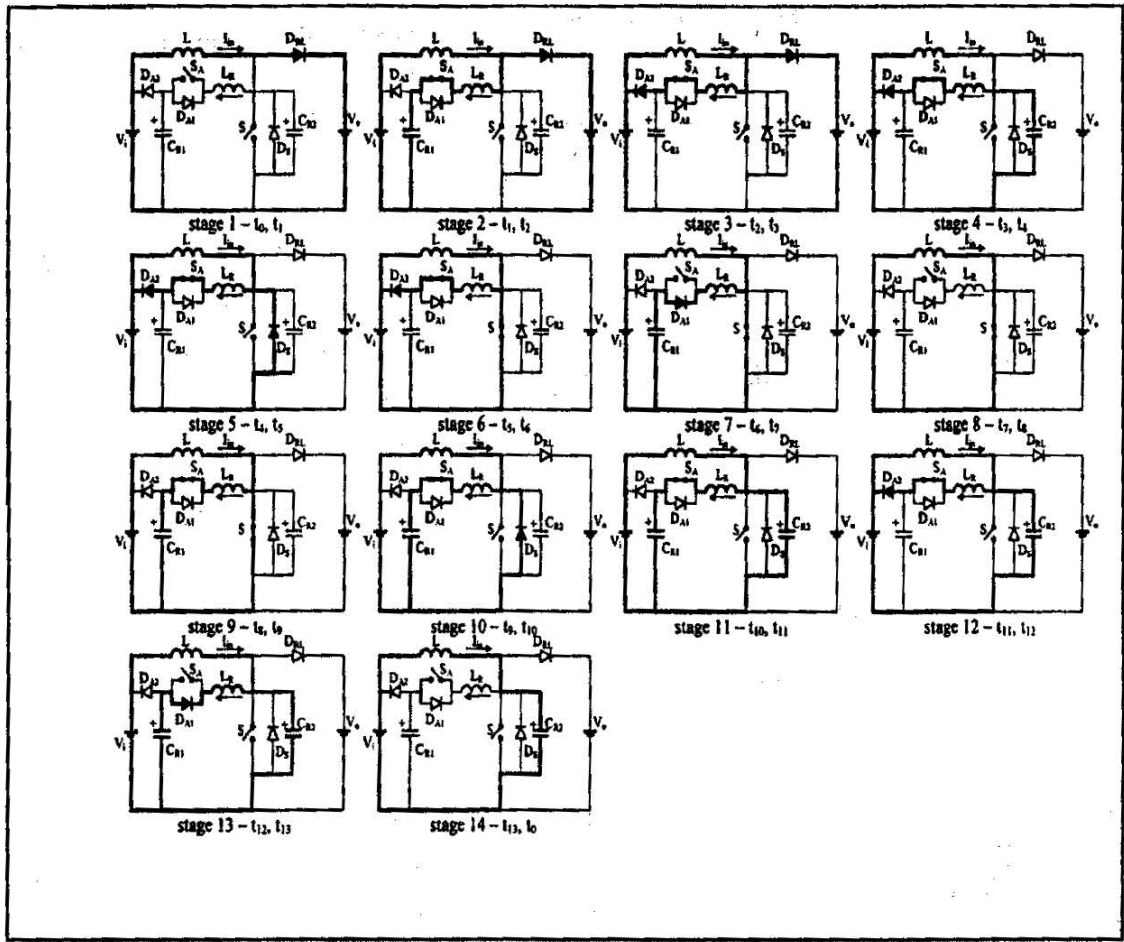


Fig.3 Operation stages of ZCZVT PWM boost converter.

2.2 Design Guidelines and an Example

This section presents a design procedure and an example to determine the resonant tank elements values of the used ZCZVT PWM Boost converter. The given converter specifications are shown in table (1),[8]:

Table-1 Converter specifications

Quantity	Value
Input Voltage ( $V_i$ )	155V
Output Voltage ( $V_o$ )	340 V
Output Power ( $P_o$ )	1000 W
Approximate Efficiency ( $\eta$ )	95%

The design procedure consists of six steps shown in table (2):

Table-2 Design procedure

step	Quantity	Symbol	Calculations
1	DC voltage conversion ratio	$K_v$	From the specifications of the converter it is possible to obtain this ratio as: $k_v = \frac{V_o}{V_i} \approx 2.2$
2	The resonant inductor	$L_R$	It is calculated to control the $di/dt$ rate and therefore, to minimize the reverse recovery of the output diode. This value was chosen equal to $40 \text{ A}/\mu\text{s}$ and then: $L_R = \frac{V_o - V_{i\min}}{di/dt} = \frac{340 - (0.9 \times 155)}{40 \times 10^6} \approx 5 \mu\text{H}$
3	The input current	$I_{in}$	Its value is defined from the specifications of converter as: $I_{in} = \frac{P_o}{\eta V_i} = \frac{1000}{0.95 \times 155} = 6.79 \text{ A}$
4	Maximum dc input current	$I_{in\max}$	Taking into account the minimum voltage, the maximum value of the input current is: $I_{in\max} = 1.25 \times \frac{P_o}{\eta \times V_{i\min}}$
5(a)	The resonant capacitors	$C_{R1}$	Its value is calculated to achieve the main switch soft turn- off condition. This capacitor can be calculated as: $C_{R1} \geq L_R \left( \frac{I_{in\max}}{V_{i\min}} \right)^2 \quad (1)$ or, $C_{R1} = k_{cl} L_R \left( \frac{I_{in\max}}{V_{i\min}} \right)^2 \quad (1')$ where $k_{cl}$ is a factor that guarantee the inequality

			<p>given in Eq.(1). Choosing <math>k_{c1}=1.3</math> and from Eq.(1'), the <math>C_{R1}</math> value is found to be:</p> $C_{R1} = 1.3 \times 5 \times 10^{-6} \left( \frac{9.43}{0.9 \times 155} \right)^2 = 29.7nF$
5(b)	The resonant capacitor	$C_{R2}$	<p>The value of this capacitor must be satisfied the achievement of the resonant transition conditions, in fact, its value is calculated based on the dc conversion ratio and the factor that guarantee the inequity given in Eq.(1). With the same steps described in [8], this value is equal to 31.185nf.</p>
6	The switching frequency	$f_s$	<p>It is interesting that the sum of the resonant time intervals involves a small fraction of the switching period, by calculations realized in Matlab<sup>®</sup> software, with the calculated parameters, the sum is found to be 4.0576<math>\mu</math>s. In these design procedures, this sum has been defined to be equal to 20 % of the switching period. Therefore, the maximum switching frequency is given by:</p> $f_s \leq \frac{20}{100 * (4.0576 * 10^{-6})} = 49.2kHz$ <p>The switching frequency was assumed equal to 40kHz.</p>

### 3 Open Loop Control Circuit

#### 3.1 Control Circuit Strategy

The open loop control circuit for the ZCZVT PWM Boost converter presented in this paper is shown in Fig.4. It is composed of Current to Pulses Conversion Circuits

(CPCC), Pulse Width Modulation Circuit (PWMC), and Gate Drive Circuit (GDC).

To expedite the development and evolution of control strategy, Mathwork's Matlab software was selected. The blocks descriptions of the simulink subsystems of Fig.4 are given in Figs.5-8.

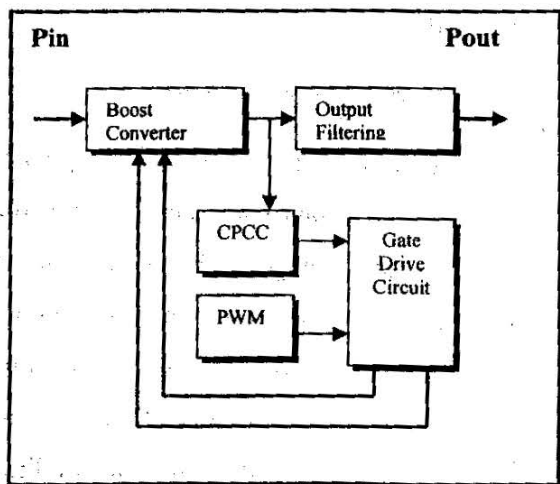


Fig.4 Block diagram of control circuit and power circuit.

**CPCC** The Current to Pulses Conversion Circuit block is shown in Fig.5 where the active switches current convert to pulses play an essential role in gate drive circuit to achieve the required soft-switching conditions.

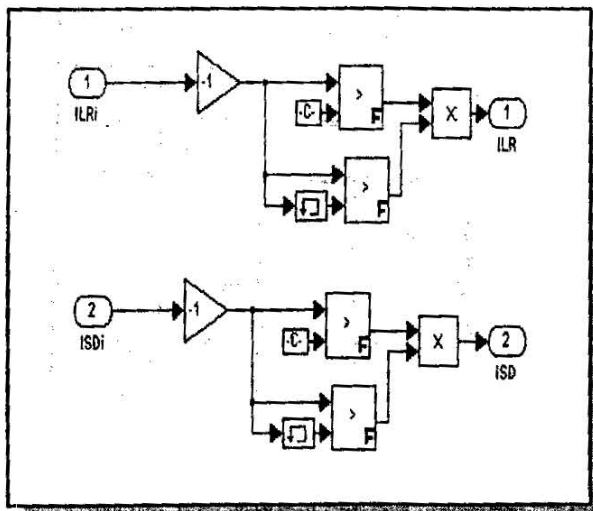


Fig.5 The simulation block diagram of CPCC.

**PWM Circuit** The Pulse Width Modulation Circuit generates pulses playing main role in generating the gate drive pulses which control the switching process of the active switches and hence, control the output voltage. Fig.6-a shows the simulation block diagram of PWM circuit. The required pulses (PWMP) obtained according to the comparison between the command signal  $V_d$  and the sawtooth signal  $Saw(t, T_s)$  are shown clearly in Fig.6-b.

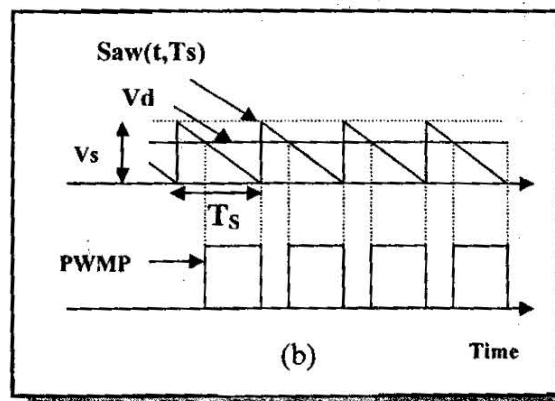
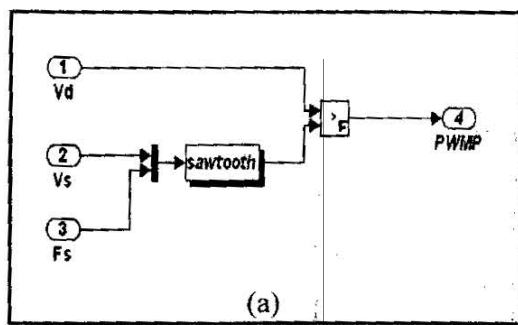
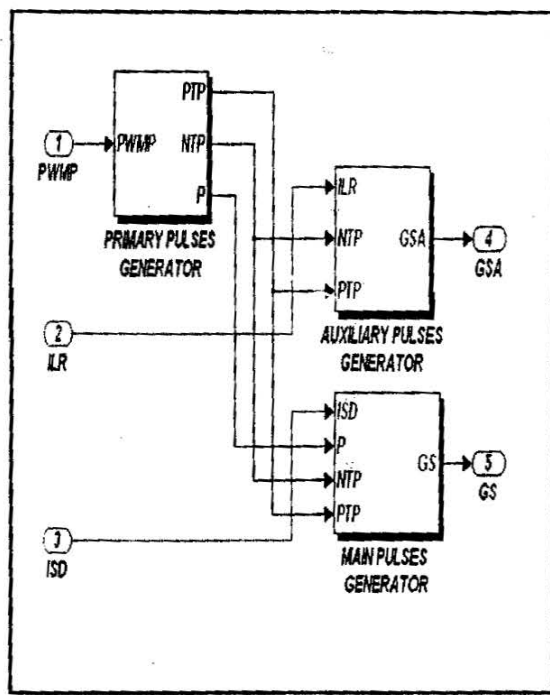


Fig.6 The PWM circuit  
(a) Simulation block diagram.  
(b) Timing diagram.

**(GDC)** The Gate Drive Circuit is designed such that the ZCZVT for the main switch at both turn-on and turn-off can be achieved, and, the ZCT at turn-on and ZCZVT at turn-off for the auxiliary switch are satisfied. The simplified diagram of the proposed gate drive circuit is shown in Fig.7, it composed of three basic subcircuits as : 1) **The primary pulses generator circuit (PPGC)**, 2) **The auxiliary pulses generator circuit (APGC)**, and 3) **The main pulses generator circuit (MPGC)**. The complete simulation diagram can be described with Fig.8.



**Fig.7** The simplified diagram of the proposed gate drive circuit.

### 3.2 The Open Loop Simulation Result

#### A) Command Voltage Range Test

The command voltage or  $V_d$  represents the most important parameter in controlling the output voltage. The range of the command voltages must be measured in accurate manner, so that the desired output voltage can be obtained while at the same time satisfying the soft-switching condition. Experimental testing using Matlab/simulation of open-loop circuit shown in Fig.4 gave the results listed in Table-3. These result show that, the output voltage changes in a wide range with the change of the command voltage ( $V_d$ ).

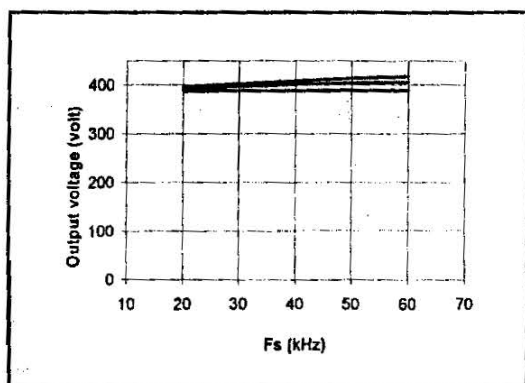
**Table-3** The relation between the command voltages and the output voltages.

$V_d$ ( Volt )	$V_o$ ( Volt )
0.9	288
1	318.7
1.1	355
1.2	401
1.3	485
1.4	533.5



## B) Frequency Test

The converter output voltage against the switching frequency for different values of the load resistor and with a selective value of the command voltage is shown in Fig.9. It is clear that there is only a small change in output voltage with a wide change in the switching frequency.



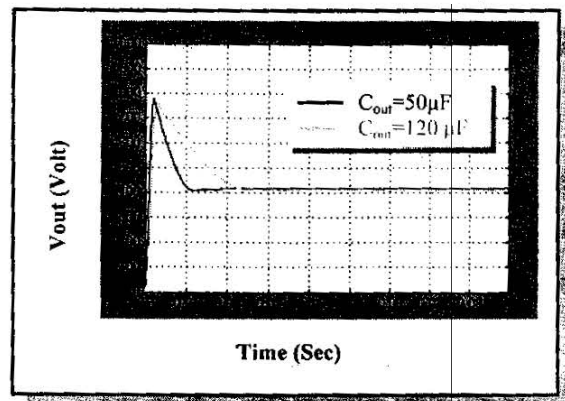
**Fig.9 The Output voltage against switching frequency for  $V_d = 1.2V$  and different Load resistances.**

## C) Transient simulation result

Figs.10-12 show a comparison of the transient performance simulation results obtained for the proposed converter due to the change of:

- Output capacitor value.
- Load resistance value, and
- Command voltage  $V_d$ .

From these simulation results, the change of the filter capacitor value has a great effect on the transient response for the output converter voltage (see Fig.10). In fact, the most important factor in choosing the value of the filter capacitor is the value of the output voltage ripple. However, there is a trade-off between the cost and size from one side and the output voltage ripple from the other.



**Fig.10 The output voltage response when output filter capacitor changed from  $50\mu F$  to  $120\mu F$ .**

Fig.11 shows the response of the control circuit for change in the magnitude of the load resistance. A change in the magnitude of the load resistances will produce a small effect in the output voltage.

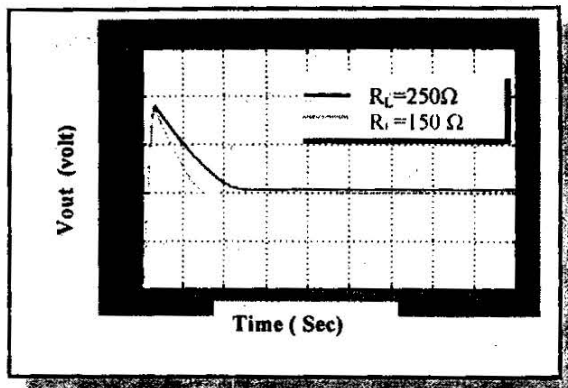


Fig. 11 The output voltage response for output resistive load change.

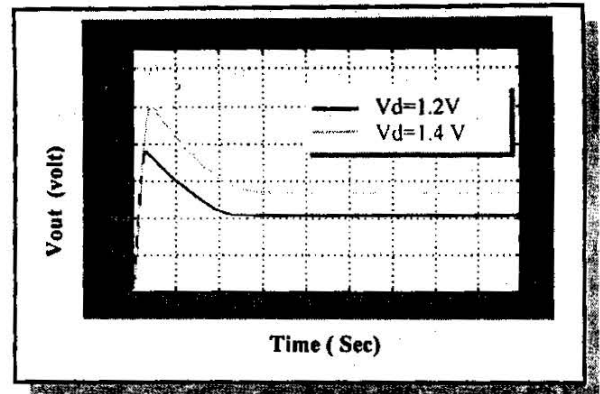


Fig. 12 The output voltage response for change in command voltage.

Fig.12 shows a comparison of the transient performance simulation result obtained from the change in a command voltage  $V_d$ . This figure shows that, the output voltage changes in a wide range with change in the command voltage  $V_d$ . So that, this parameter represents the most important one for controlling the proposed converter topology.

#### 4. Closed Loop Operation

Control of complex and nonlinear system is an important challenging task and various strategies have appeared in recent literature to deal with nonlinearity and strong coupling of dynamic systems. The Proportional-Integral-Derivative (PID) is a popular control method extensively used in an industrial set up. The advantages of PID controller include its simple structure along with robust performance in a wide range of operating conditions [9,10].

However, the design of a PID controller is generally based on the assumption of exact knowledge about the system. This assumption is often not valid since the development of model of any practical system may not include precise information of factors such as the effect of parasitic elements and uncertainty arising from any of the sources.

In recent years, there has been an increasing interest in the utilization of unconventional control strategies such as neural network and fuzzy controller. These control methods derive their advantages from the fact that they do not use any mathematical model of the system. Instead they use input-output relations (Neural Network) or heuristic knowledge (Fuzzy Logic) about the system. This work investigates the use of fuzzy logic to control ZCZVT boost converter based on operator experience and trial and error iteration.

#### 4.1 Problem Formulation and Approach

The control problem considered in this paper is to control the switching process such that the suitable output voltage can be obtained at the same time of satisfying the Soft-Transition conditions for switching devices (IGBTs). This can be done by controlling the command voltage ( $V_d$ ) for PWM circuit which directly controls the gate pulses of active switches and hence, the quality of the output voltage. Fuzzy Logic approach has been considered in the paper, the inputs to the fuzzy logic are **error** in output voltage (the difference in desired output voltage and current output voltage) and the change of that **error**. The output of the controller is the controlled command voltage ( $V_d$ ).

The close loop simulation results that describe the performance of the proposed converter with this control strategy due to different effects (Input voltage changes, Load variations and Output reference changes) are also included, and discussed.

#### 4.2 The Proposed Control Strategy

Fig.13 shows the simulation block diagram of the proposed Fuzzy Proportional Derivative + Integral FPD+I controller, which uses the output voltage error,  $e(t)$ , into a PD fuzzy scheme combined with an integral component needed for the zero steady state error. The PD controller provides the "coarse" control actions but it is unable to eliminate the steady-state error. The integration provides the additional signal to correct the error.

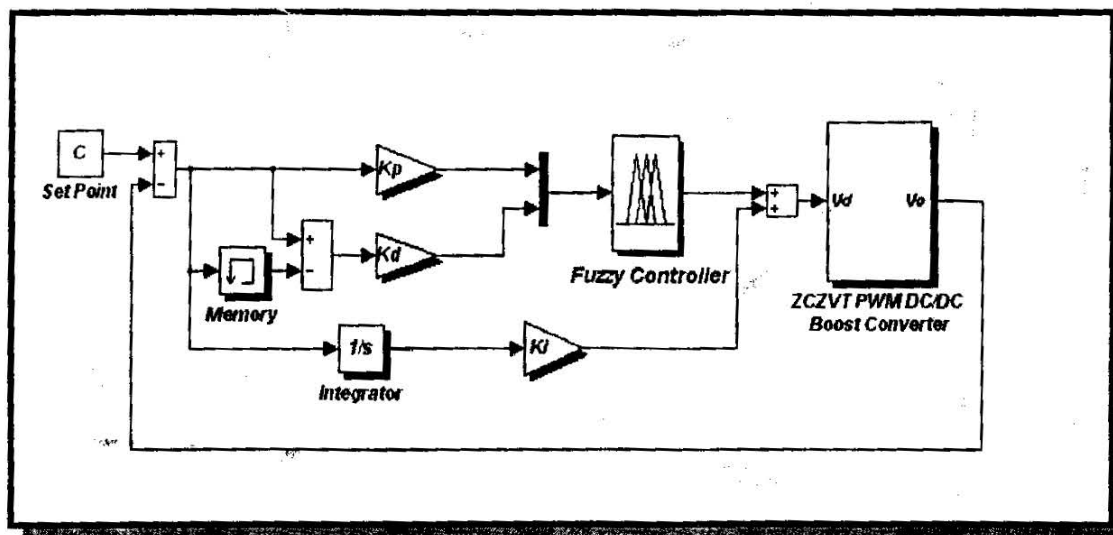


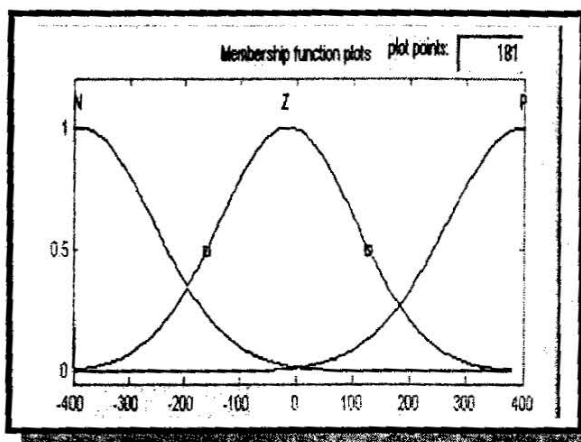
Fig.13 The simulation block diagram of fuzzy PD+I controller.

### 4.3 Design of FPD+I Controller

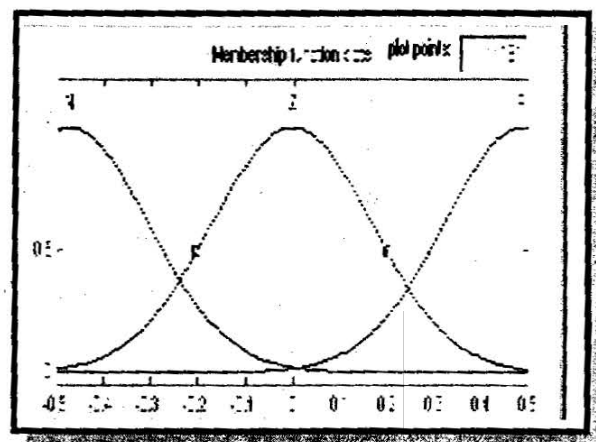
The fuzzy logic controller is made of three components:

❖ **Input/Output Interface** Input interface consist of fuzzification unit which converts the inputs of the controller into membership grades of fuzzy sets with the help of

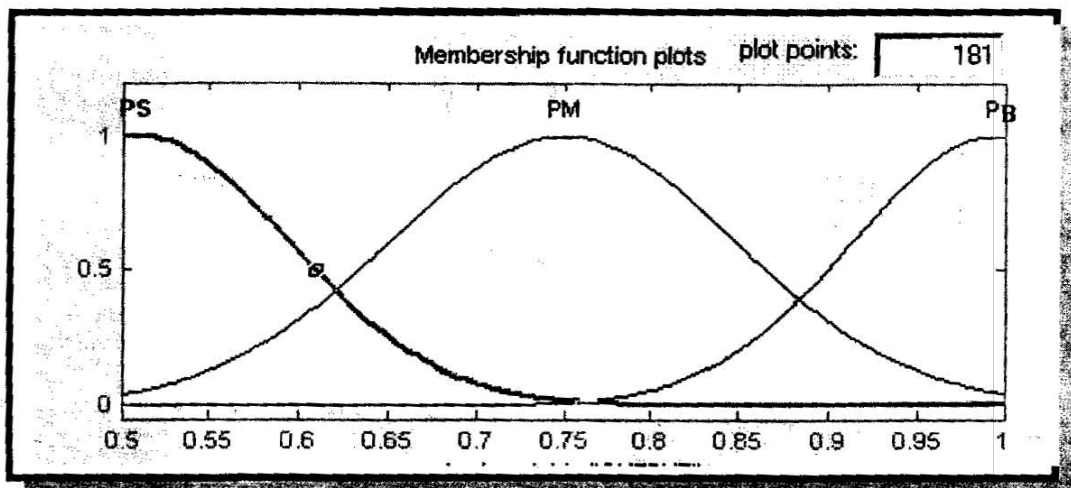
membership functions. Output interface consist of defuzzification unit which converts membership grades of outputs into crisp number. The nonlinear membership functions of bell shape are used here for input as well as output variables as shown in Fig. 14.



(a) error



(b) errordot



(c) comvoltage

Fig.14 Membership functions for inputs (error and errordot) and output (comvoltage).

❖ **Knowledge or rule base** comprises of data base and fuzzy control rule base which characterizes the desired output response applied by means of a set of control rules. Based on the usual action of a PD cell, by looking at it's output range as a function of the inputs range, a rule based inference is chosen for each consequent. The respective rules with **linguistic phase plane (tabular linguistic)** format are shown in Table-4. While Fig.15 is a mesh plot of an approach relationship between error  $e(t)$ , and its rate  $\dot{e}(t)$  on the input side, and controller output voltage (Vd) on the output side.

❖ **Reasoning/Inference Mechanism** is the kernel of fuzzy logic controller which has the capacity of simulating the human decision making mechanism based on fuzzy concepts and fuzzy control actions.

#### 4.4 Closed Loop Simulation Results

The results of the simulation studies were obtained using a detailed simulink model of the controlled converter. The simulation includes the close loop converter model of Fig.13. Three tests, which cover three basic performance areas, i.e., duty cycle, load and line regulations are carried out to evaluate the controller performance.

Table-4 The fuzzy control rule base.

$\begin{matrix} & e \\ \dot{e} & \end{matrix}$	N	Z	P
N	PB	PB	PM
Z	PM	PM	PM
P	PM	PS	PS

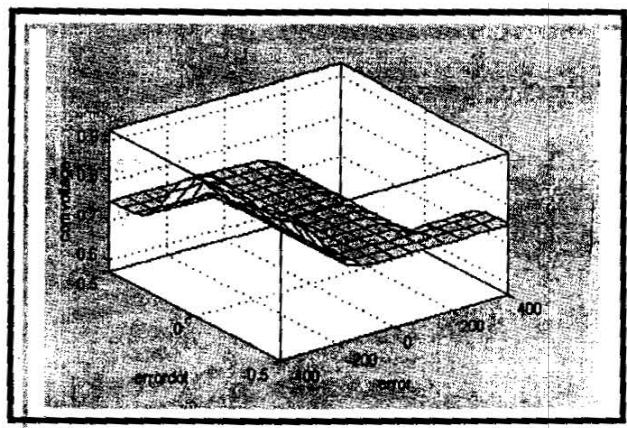


Fig.15 Fuzzy controller surface.

❖ **Duty Cycle Regulation Results** The transients caused by sudden change in duty cycle were captured as clearly shown in Fig.16. This figure show that FPD+I controller has a good performance during the sudden change of the duty cycle.

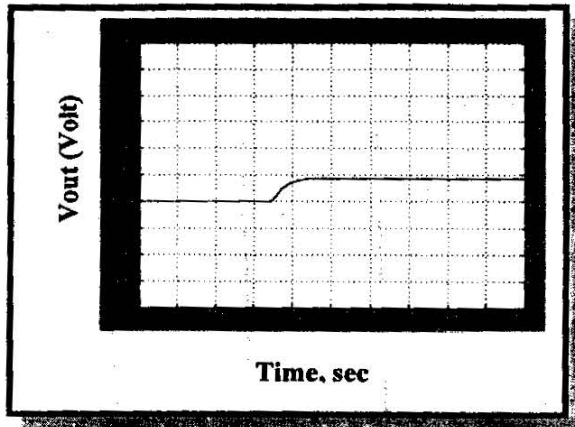


Fig.16 The converter output voltage response for sudden change of the set point from 400V to 485V.

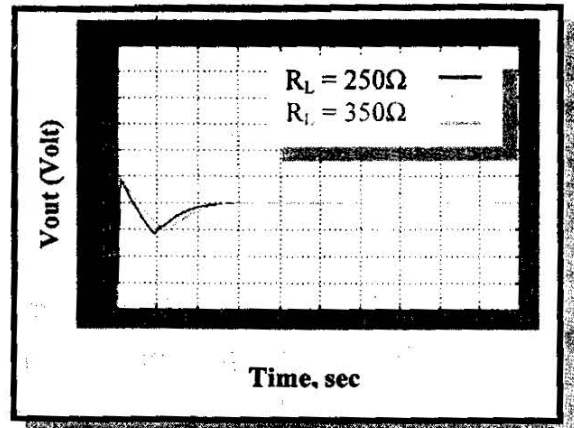


Fig.17 The converter output voltage response for different load resistances.

❖ **Load Regulation Results** Fig.17 gives the transients caused by the sudden change in the load, it can be seen clearly that, the converter is robust against the change of the load with FPD+I controller.

❖ **Line Regulation Results** In order to evaluate the dynamic performance of the system under wide operating range, the FPD+I controller is applied to regulate boost converter under different input voltages without changing controller parameters. Fig.18 shows the simulation result of the converter output voltage when the input voltage is increased to 200V. It is shown that the dynamic performance of the FPD+I due to the sudden change in input voltage has some oscillation emerges

during the transition period, but the controller can correct its operation after a small period (less than 0.1 sec.).

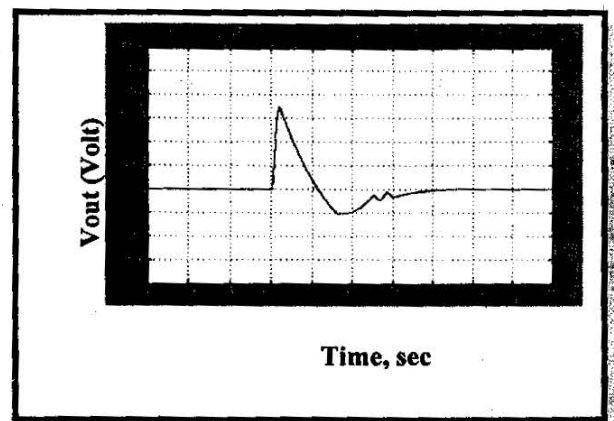


Fig.18 The output voltage response of the FLC due to sudden change in the input voltage from 155V to 200V.

## 5 Conclusion

A new control circuit is designed to ensure the soft-switching of the used converter. The open-loop operation has been described. Simulation results for control strategy are discussed. Also, the paper introduces fuzzy control as a technique for significantly improving the performance of the converter. The advantage of fuzzy controller could be seen in its good robustness and adaptability to input voltage changes, load variations and output reference changes. The results presented show that the present FPD-I control methodology is effective and the control behaviors exhibit our predicted characteristics.

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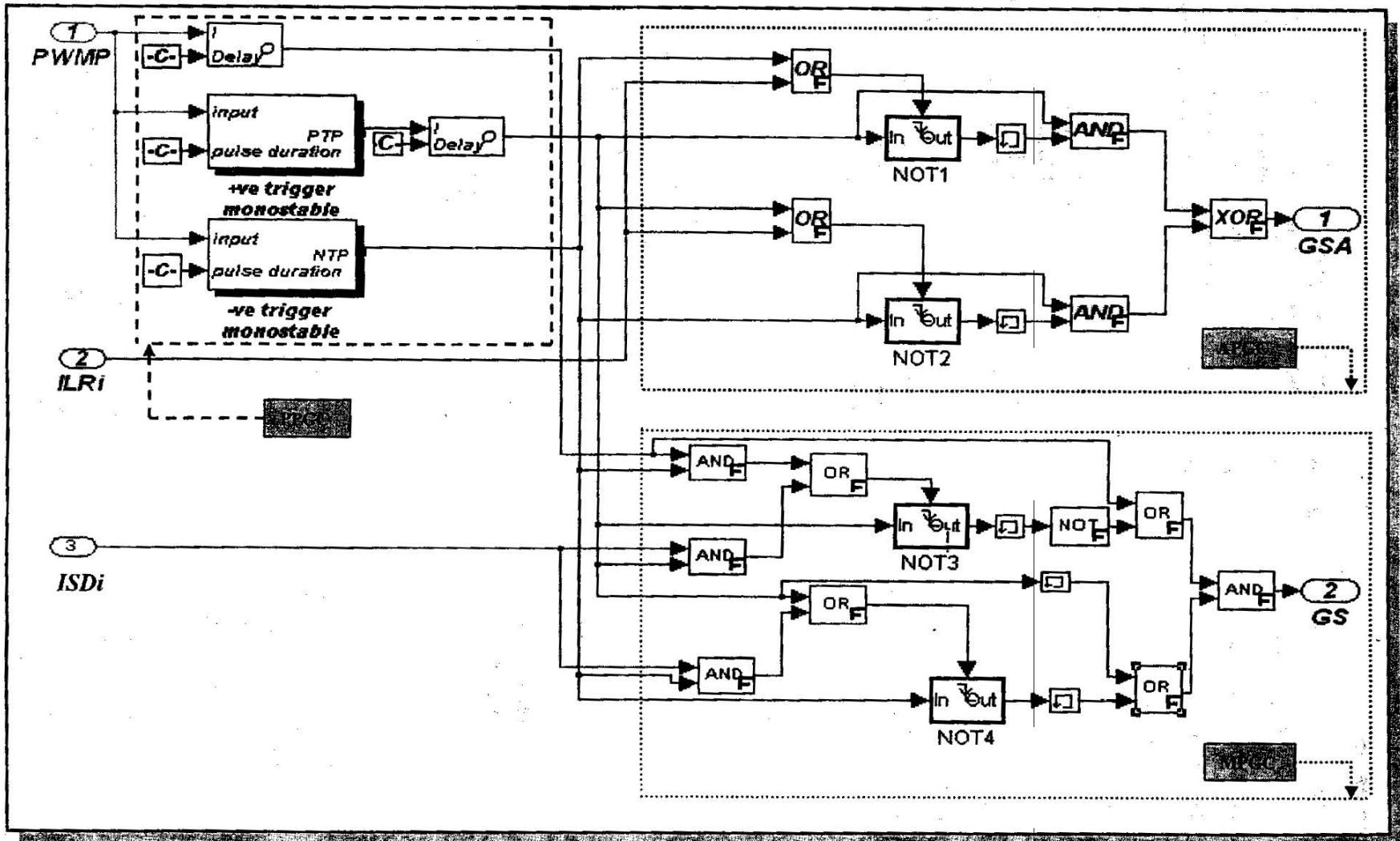


Fig.8 The complete simulation diagram of the proposed gate drives circuit.